



CONNECTION DIAGRAM and PIN DEFINITION - 8 BIT MICROPROCESSOR - M 380

V _{CC}	1	V _{CC}	20	DB0N	15	NC	AD0A3	17	AD0A3
SYNC	2	V _{CC}	19	DB0N	16	NC	AD0A4	18	AD0A4
CLOCK	3	PPOP	18	DB0N	17	NC	AD0A5	19	AD0A5
V _{SS}	4	WEQZ	20	DB0N	18	NC	AD0A6	20	AD0A6
V _{SS}	5	ADSL	21	DB0N	19	NC	AD0A7	21	AD0A7
DB8N	6	DBDI	22	DB0N	20	NC	AD0A8	22	AD0A8
DB7N	7	NC	23	DB0N	21	NC	AD0A9	23	AD0A9
DB6N	8	NC	24	DB0N	22	NC	AD0B0	24	AD0B0
DB5N	9	NC	25	DB0N	23	NC	AD0B1	25	AD0B1
DB4N	10	NC	26	DB0N	24	NC	AD0B2	26	AD0B2
DB3N	11	NC	27	DB0N	25	NC	AD0B3	27	AD0B3
DB2N	12	NC	28	DB0N	26	NC	AD0B4	28	AD0B4
DB1N	13	NC	29	DB0N	27	NC	AD0B5	29	AD0B5
PBO8N	14	AD0A3	30	DB0N	28	NC	AD0B6	30	AD0B6
PBO7N	15	AD0A4	31	DB0N	29	NC	AD0B7	31	AD0B7
PBO6N	16	AD0A5	32	DB0N	30	NC	AD0B8	32	AD0B8
PBO5N	17	AD0A6	33	DB0N	31	NC	AD0B9	33	AD0B9
PBO4N	18	AD0A7	34	DB0N	32	NC	AD0C0	34	AD0C0
PBO3N	19	AD0A8	35	DB0N	33	NC	AD0C1	35	AD0C1
PBO2N	20	AD0A9	36	DB0N	34	NC	AD0C2	36	AD0C2
		AD0B0	37	DB0N	35	NC	AD0C3	37	AD0C3
		AD0B1	38	DB0N	36	NC	AD0C4	38	AD0C4
		AD0B2	39	DB0N	37	NC	AD0C5	39	AD0C5
		AD0B3	40	DB0N	38	NC	AD0C6	40	AD0C6

- SYNC Initial reset/synchronization input
- CLOCK System clock (input)
- DAB 8N DAB 1N 8 bit bidirectional data-bus
- PBO 8N PBO 5N 4 bit input-output peripheral-bus
- PBO 4N PBO 1N 4 bit input peripheral bus
- ADB 6X ADB 1X 6 bit address bus (outputs)
- DBDI Data bus direction
- ADSL Address/data select } 4 control
- WEQZ Write enable a or Z } lines (outputs)
- PPOP Push/pop operation
- X Data true if logic level is 1
- N Data true if logic level is 0

LP8000 LOGIC PROCESSOR

Pin Connections

1	Vcc	21	Peripheral Bus 1
2	Power on Reset	22	Address Bus 1
3	Clock	23	" " 2
4	Not Used	24	" " 3
5	" "	25	" " 4
6	Data Bus 8	26	" " 5
7	" " 7	27	" " 6
8	" " 6	28	Not Used
9	" " 5	29	" "
10	" " 4	30	" "
11	" " 3	31	" "
12	" " 2	32	" "
13	" " 1	33	" "
14	Peripheral Bus 8	34	" "
15	" " 7	35	CIO
16	" " 6	36	CDA
17	" " 5	37	CQZ
18	" " 4	38	CRA
19	" " 3	39	Vgg
20	" " 2	40	Vgi